What is Claimed is:

[c1] A method of performing back-to-back read and write memory operations to a same DRAM bank, said method comprising:

articulating between reading data on a first bank during successive first bank read cycles and writing data to a second bank during successive second bank write cycles;

cycling between reading data on said second bank during successive second bank read cycles and writing data to said first bank during successive first bank write cycles; and

performing a refresh cycle on said first and second bank, wherein said first bank write cycles lag said first bank read cycles, and

wherein said second bank write cycles lag said second bank read cycles.

[c2] The method of claim 1, wherein said step of articulating comprises:

reading data on said first bank during said first bank read cycle;

writing data to said second bank during said second bank write cycle;

reading additional data on said first bank during said first bank read cycle; and

writing additional data to said second bank during said second bank write cycle.

[c3] The method of claim 1, wherein said step of cycling comprises:

reading data on said second bank during said second bank read cycle;

writing data to said first bank during said first bank write cycle;

reading additional data on said second bank during said second bank read cycle; and

writing additional data to said first bank during said first bank write cycle.

[c4] The method of claim 1, wherein said refresh cycle is performed on said first bank after said step of writing additional data to said second bank.

[c5] The method of claim 1, wherein said refresh cycle is performed on said second bank after said step of writing additional data to said first bank.

[c6] The method of claim 1, wherein said read and write memory operations

constantly swap between said read and write cycles.

[c7] The method of claim 1, wherein said read and write memory operations constantly swap between said first and second bank.

[c8] The method of claim 1, wherein said read and write memory operations occur in a frequency of 2n times within the same bank.

[c9] The method of claim 1, wherein said lag comprises at least two write cycles.

[c10] A method of performing back-to-back read and write memory operations to a same DRAM bank, said method comprising:

reading data on a first bank during an nth read cycle;
writing data to a second bank during a nth write cycle;
reading data on said first bank during a (nth + 1) read cycle;
writing data to said second bank during a (nth + 1) write cycle;
refreshing data on said first bank;
reading data on said second bank during a (nth + 2) read cycle;
writing data to said first bank during a (nth + 2) write cycle;
reading data on said second bank during a (nth + 3) read cycle;
writing data to said first bank during a (nth + 3) write cycle; and
refreshing data on said second bank.

[c11] The method of claim 10, wherein said read and write memory operations occur in a frequency of 2n times within the same bank.

[c12] A method of accessing banks of dynamic random access memory (DRAM) memory, said method comprising:

applying a first group of access requests to a first DRAM memory bank during a first time period, wherein at least one of said access requests is buffered; and
applying a second group of access requests to a second DRAM memory bank during a second time period,
wherein, access requests that are buffered during said first time period are executed during said second time period.

[c13] The method of claim 12, wherein said first group of access requests comprises read and write memory operations constantly swapping between read and write cycles.

[c14] The method of claim 13, wherein said read and write memory operations occur in a frequency of 2n times within each of said first DRAM memory bank.

[c15] The method of claim 12, wherein said second group of access requests comprises read and write memory operations constantly swapping between read and write cycles.

[c16] The method of claim 15, wherein said read and write memory operations occur in a frequency of 2n times within each of said second DRAM memory bank.

[c17] A multi-bank memory circuit operable to allow back-to-back read and write memory operations to be performed on a same DRAM bank, said circuit comprising:

a plurality of independently addressable DRAM memory banks;

a refresh counter connected to said DRAM memory banks, said refresh counter operable to send an address to each said DRAM memory banks;

a read register connected to said DRAM memory banks, said read register operable to send a read address to each said DRAM memory banks;

a write register connected to said DRAM memory banks, said write register operable to send a write address to each said DRAM memory banks;

an address comparator connected to said read register and said write register, said address comparator operable to compare said read and write addresses; and

a plurality of buffers connected to said DRAM memory banks, wherein said buffers artificially reduces an apparent cycle time of said DRAM memory banks.

[c18] The circuit of claim 17, further comprising a partition array in each said DRAM memory banks.

[c19] The circuit of claim 18, wherein said address comparator monitors said write

registers to determine if said write address has been stored in said partition array.

[c20] The circuit of claim 17, wherein said refresh counter is operable to track all addresses to be refreshed.

[c21] The circuit of claim 17, wherein said read and write memory operations constantly swap between a read and write cycle.

[c22] The circuit of claim 17, wherein said plurality of DRAM memory banks comprises a first and second DRAM memory bank.

[c23] The circuit of claim 22, wherein said first DRAM memory bank is adapted to receive a first group of access requests during a first time period, wherein said second DRAM memory bank is adapted to receive a second group of access requests during a second time period, wherein at least one of said first access requests is buffered, and wherein said access requests that are buffered during said first time period are executed during said second time period.

[c24] The circuit of claim 22, wherein said read and write memory operations constantly swap between said first and second DRAM memory bank.

[c25] The circuit of claim 17, wherein said read and write memory operations occur in a frequency of 2n times within the same bank.

[c26] The circuit of claim 17, further comprising an input clock operatively connected to said read and write registers, said input clock operable to capture data from said read and write registers.

[c27] A program storage device readable by machine, tangibly embodying a program of instructions executable by said machine to perform a method of performing back-to-back read/write memory operations to a same DRAM bank, said method comprising:

articulating between reading data on a first bank during successive first bank read cycles and writing data to a second bank during successive second bank write cycles;

cycling between reading data on said second bank during successive

second bank read cycles and writing data to said first bank during successive first bank write cycles; and

performing a refresh cycle on said first and second bank,

wherein said first bank write cycles lag said first bank read cycles, and

wherein said second bank write cycles lag said second bank read cycles.

[c28] The program storage device of claim 27, wherein said step of articulating comprises:

reading data on said first bank during said first bank read cycle;

writing data to said second bank during said second bank write cycle;

reading additional data on said first bank during said first bank read cycle; and

writing additional data to said second bank during said second bank write cycle.

[c29] The program storage device of claim 27, wherein said step of cycling comprises:

reading data on said second bank during said second bank read cycle;

writing data to said first bank during said first bank write cycle;

reading additional data on said second bank during said second bank read cycle; and

writing additional data to said first bank during said first bank write cycle.

[c30] The program storage device of claim 27, wherein said refresh cycle is performed on said first bank after said step of writing additional data to said second bank.

[c31] The program storage device of claim 27, wherein said refresh cycle is performed on said second bank after said step of writing additional data to said first bank.

[c32] The program storage device of claim 27, wherein said read and write memory operations constantly swap between said read and write cycles.

[c33] The program storage device of claim 27, wherein said read and write memory operations constantly swap between said first and second bank.

[c34] The program storage device of claim 27, wherein said read and write memory operations occur in a frequency of 2n times within the same bank.

[c35] The program storage device of claim 27, wherein said lag comprises at least two write cycles.